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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/712,426	11/13/2003	Chang-Hyun Lee	5649-1181	9949
20792	7590	04/27/2005		EXAMINER
MYERS BIGEL SIBLEY & SAJOVEC PO BOX 37428 RALEIGH, NC 27627				HUYNH, ANDY
			ART UNIT	PAPER NUMBER
			2818	

DATE MAILED: 04/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	on
	10/712,426	LEE, CHANG-HYUN	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 11 April 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-20 and 40 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1,7-11 and 19 is/are rejected.
- 7) Claim(s) 2-6,12-18,20 and 40 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 13 November 2003 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 03/07/05
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____

DETAILED ACTION

Election/Restrictions

In the Response to Election Requirement and second Preliminary Amendment, filed April 11, 2005, Applicant's election with traverse of Species I which is drawn to claims 1-6, claims 21-39 have been canceled, claims 1-3, 5 and 6 are amended, and new claim 40 is added is acknowledged.

Response to Arguments

Applicant's remarks, see the Response to Election Requirement and second Preliminary Amendment, filed April 11, 2005, with respect to the election/restrictions requirement set forth in the Office Action mailed March 14, 2005 have been fully considered and are persuasive. The election/restrictions requirement of claims 1-20 has been withdrawn. Accordingly, claims 1-20 and 40 are currently pending in this application.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) based on an application filed in REPUBLIC OF KOREA, 2003-01566 on 01/10/2003.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed on 03/07/2005. The references cited on the PTOL 1449 form have been considered.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 7-9, 11 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Kume et al. (USP: 5,188,976 hereinafter referred to as "Kume").

Regarding claim 1, Kume discloses in Figs. 6-17 and the corresponding texts as set forth in column 7, line 40-column 13, line 21, a non-volatile memory device comprises:

a substrate 11;

a plurality of isolation layers 14 on the substrate that define a plurality of active regions

therebetween;

a charge storage insulator/a composite of silicon oxide films 18, 20 and a silicon nitride 19 on the plurality of active regions and the plurality of isolation layers; and

a plurality of gate lines 21 on the charge storage insulator/the composite of silicon oxide films and crossing over the plurality of active regions (Fig. 17).

Regarding claim 7, Kume discloses in Figs. 6-17 and the corresponding texts as set forth in column 7, line 40-column 13, line 21, a non-volatile memory device comprises:

a substrate 11 having a cell region/MEMORY TRANSISTOR AREA, a high voltage region/FIRST PERIPHERAL CIRCUIT MOS TRANSISTOR AREA and a low voltage region/SECOND PERIPHERAL CIRCUIT MOS TRANSISTOR AREA (Fig. 17);

a plurality of trench isolation layers 14 on the substrate that define a plurality of first active regions in the cell region/MEMORY TRANSISTOR AREA, a plurality of second active regions in the high voltage region/FIRST PERIPHERAL CIRCUIT MOS TRANSISTOR AREA and a plurality of third active regions in the low voltage region/SECOND PERIPHERAL CIRCUIT MOS TRANSISTOR AREA;

a charge storage insulator/a composite of silicon oxide films 18, 20 and a silicon nitride 19 on the plurality of first active regions and the plurality of trench isolation layers in the cell region of the device;

a plurality of gate lines 21 on the charge storage insulator/the composite of silicon oxide films and crossing over the plurality of trench isolation layers in the cell region of the device.

Regarding claim 8, Kume discloses in Fig. 17 the device further comprises:

a high voltage gate electrode 40 of the FIRST PERIPHERAL CIRCUIT MOS TRANSISTOR AREA crossing over each of the plurality of second active regions and a first insulation layer 38 interposed between the high voltage gate electrode and each of the plurality of second active regions.

a low voltage gate electrode 40 of the SECOND PERIPHERAL CIRCUIT MOS TRANSISTOR AREA crossing over each of the plurality of third active regions and a second insulation layer 39 interposed between the low voltage gate electrode and each of the plurality of third active regions.

Regarding claim 9, Kume discloses in Fig. 17 a top surface of each of the plurality of trench isolation layers is disposed farther above the substrate than a top surface of each of the plurality of first, second and third active regions.

Regarding claim 11, Kume discloses in Fig. 17 the first insulation layer 38 is thicker than the second insulation layer 39.

Regarding claim 19, Kume discloses in Figs. 6-17 and the corresponding texts as set forth in column 7, line 40-column 13, line 21, a non-volatile memory device comprises:

a substrate 11 having a cell region/MEMORY TRANSISTOR AREA, a high voltage region/FIRST PERIPHERAL CIRCUIT MOS TRANSISTOR AREA and a low voltage region/SECOND PERIPHERAL CIRCUIT MOS TRANSISTOR AREA (Fig. 17);

a plurality of device isolation layers 14 on the substrate that define a plurality of first active regions in the cell region/MEMORY TRANSISTOR AREA, a second active region in the high voltage region/FIRST PERIPHERAL CIRCUIT MOS TRANSISTOR AREA and a third active region in the low voltage region/SECOND PERIPHERAL CIRCUIT MOS TRANSISTOR AREA;

a charge storage insulator disposed on the first active regions and the plurality of device isolation layers wherein the charge storage insulator comprises a lower oxide layer 18, a charge trapping layer 19 and an upper oxide layer 20;

a plurality of gate lines 21 on the charge storage insulator that cross over the plurality of device isolation layers in the cell region;

a first gate electrode 40 crossing over the second active region of the FIRST PERIPHERAL CIRCUIT MOS TRANSISTOR AREA;

a second gate electrode 40 crossing over the third active region the SECOND PERIPHERAL CIRCUIT MOS TRANSISTOR AREA;

a first insulation layer 38 interposed between the first gate electrode and the second active region; and

a second insulation layer 39 interposed between the second gate electrode and the third active region.

Claim 1 is also rejected under 35 U.S.C. 102(e) as being anticipated by Choi et al. (KP 2002-0094505 dated 12/18/2002 hereinafter referred to as “Choi”).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention “by another,” or by an appropriate showing under 37 CFR 1.131.

Choi discloses in Fig. 7 and the corresponding texts as set forth in the English Abstract, a non-volatile memory device comprises:

a substrate 100;
a plurality of isolation layers 161 on the substrate that define a plurality of active regions therebetween;
a charge storage insulator formed of a tunnel oxide layer 110, a nitride layer 120 and a blocking oxide layer 130 on the plurality of active regions and the plurality of isolation layers; and
a plurality of gate lines 300 on the charge storage insulator and crossing over the plurality of active regions.

Claim 1 is also rejected under 35 U.S.C. 102(e) as being anticipated by Cho et al. (KP 2003-0001088 dated 01/06/2003 hereinafter referred to as “Cho”).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention “by another,” or by an appropriate showing under 37 CFR 1.131.

Cho discloses in Figs. 6 and 7 and the corresponding texts as set forth in the English Abstract, a non-volatile memory device comprises:

a substrate 100;

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a plurality of isolation layers 101 on the substrate that define a plurality of active regions 103 therebetween;

a charge storage insulator formed of a tunnel oxide layer 152, a charge storage layer 154 and a blocking insulating layer 156 on the plurality of active regions and the plurality of isolation layers; and

a plurality of gate lines 140 on the charge storage insulator and crossing over the plurality of active regions.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kume et al. (USP: 5,188,976 hereinafter referred to as "Kume").

Kume discloses the all claimed limitations as above except for the charge storage insulator including an insulating metal oxide layer. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the charge storage insulator including an insulating metal oxide layer, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Allowable Subject Matter

Claims **2-6, 12-18, 20 and 40** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations.

Regarding claims **2-6 and 40**, the prior art of record, taken alone or in combination, fails to teach or suggest the non-volatile memory device further comprises a plurality of conductive patterns disposed between at least some of the gate lines that penetrate the charge storage insulator to electrically connect with at least some of the plurality of active regions as recited in claim **40**.

Regarding claims **12, 13 and 16**, the prior art of record, taken alone or in combination, fails to teach or suggest the non-volatile memory device wherein the first insulation layer comprises a first oxide layer and a lower oxide layer and wherein the second insulation layer comprises a second oxide layer and a lower oxide layer as recited in claim **12**. Regarding claims **14 and 15**, the prior art of record, taken alone or in combination, fails to teach or suggest the non-volatile memory device wherein the first insulation layer comprises a first oxide layer, a lower oxide layer and a second oxide layer and wherein the second insulation layer comprises the lower oxide layer and the second oxide layer as recited in claim **14**. Regarding claims **17 and 18**, the prior art of record, taken alone or in combination, fails to teach or suggest the non-volatile memory device wherein the first insulation layer comprises a first oxide layer and a second oxide layer and wherein the second insulation layer comprises the second oxide layer as recited in claim **17**. And regarding claim **20**, the prior art of record, taken alone or in combination, fails to teach or suggest the non-volatile memory device wherein the plurality of gate lines include a

plurality of word lines disposed in a word line portion of the cell region, and a ground selection gate line and a string selection gate line that are disposed in a selection gate portion of the cell region and wherein the lower oxide layer of the charge storage insulator is thinner under the plurality of word lines than the lower oxide layer of the charge storage insulator is under the ground selection gate line and the string selection gate line.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

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system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Andy Huynh

Ah

Patent Examiner

04/23/05